**LAB 7**

**Universal Gates Introduction and Implementation**

**Equipment:**

Explorer Board

**Software:**

Circuit Maker, Waveforms

**Components:**

IC Type 7400 QUAD two input NAND gate

IC Type 7402 QUAD two input NOR gate

IC Type 7404 Hex Inverters (NOT gate)

IC Type 7408 Quadruple two input AND gates

IC Type 7432 Two input OR gate

**Description:**

**Karnaugh map (K-map)**

The K-map is a method to simplify Boolean expressions. K-Map is a grid-like representation of a truth table that gives more insight. The required Boolean results are transferred from a truth table onto a two-dimensional grid where the cells are ordered in gray code and each cell position represents one combination of input conditions, while each cell value represents the corresponding output value. Optimal groups of 1s or 0s are identified, which represent the terms of a canonical form of the logic in the original truth table. These terms can be used to write a minimal Boolean expression representing the required logic.

Karnaugh maps are used to simplify real-world logic requirements so that they can be implemented using a minimum number of physical logic gates. A sum-of-products can always be implemented using AND gates feeding into an OR gate, and a product-of-sums expression leads to OR gates feeding an AND gate.

The minimization will result in reduction of the number of gates (resulting from less number of terms) and the number of inputs per gate (resulting from less number of variables per term). The minimization will reduce cost and power consumption of the logic circuit.

**Universal Gates**

The design of a combinational circuit starts from the specification of the problem and culminates in a logic diagram that describes a logic diagram. The procedure involves the specification, formulation, optimization, & technology mapping.

Technology mapping is actually transformation of logic diagram to a new diagram using the available implementation technology. Typically, NAND and NOR gates are more desirable to use in technology mapping due to the following reasons:

1) NAND and NOR gates are said to be universal gates where universal gate is a gate which can implement any Boolean function without needing any other type of gate.

2) Using universal gate in technology mapping may further reduce cost of optimized logic diagram.

3) Universal gates are easier to fabricate with electronic components.

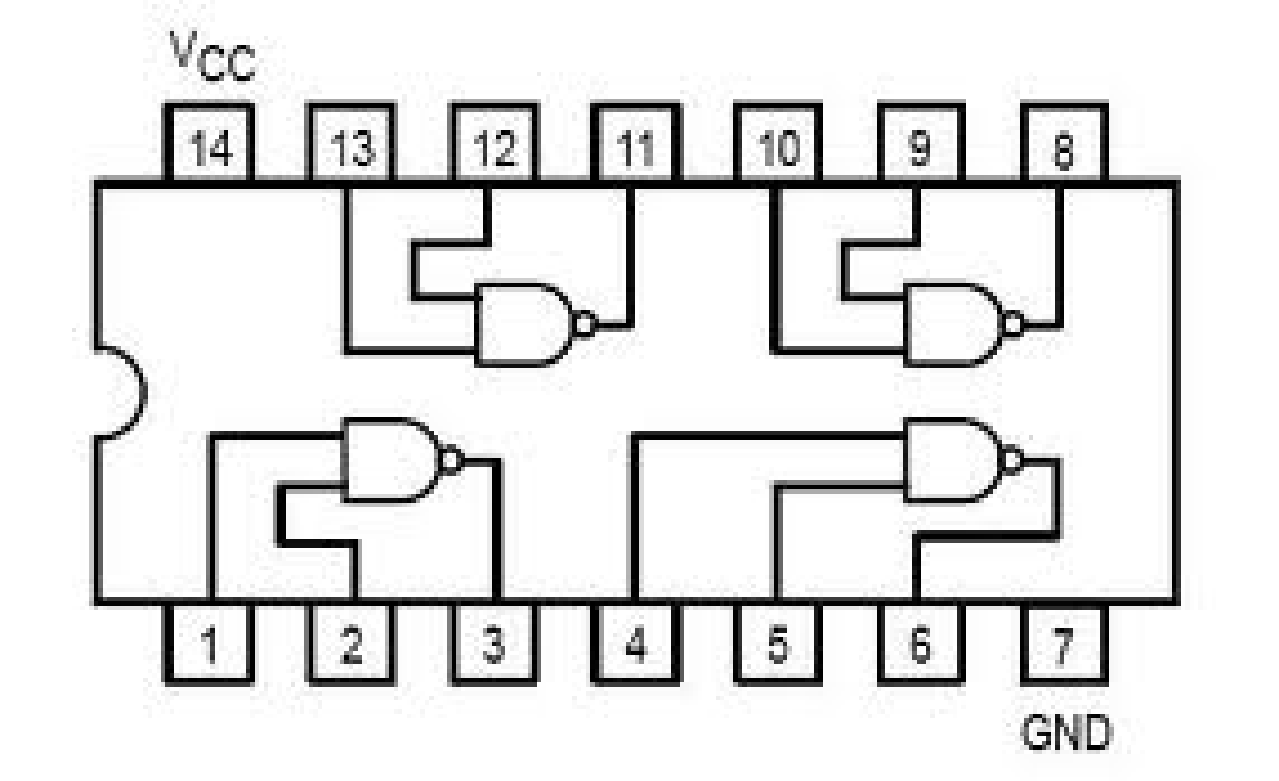
A convenient way to implement a Boolean function with NAND gates only (NAND-NAND implementation) is to begin with the optimized logic diagram of the circuit consisting of AND, OR and NOT gates. The function is converted to pure NAND logic by replacing each gate in logic diagram with its representation using NAND gates only as shown in figure 1. After that, all inverter pairs are cancelled. The same conversion procedure is applied to implement a Boolean function with NOR gates only (NOR-NOR implementation).

|  |  |
| --- | --- |
| Using NAND gate | Using NOR gate |
|  |  |
| AND ( ) | |
|  |  |
| OR ( ) | |
|  |  |
| NOT ( ) | |

**Figure 1**

In this experiment, we will use 74LS00 and 74LS02 ICs for NAND-NAND & NOR-NOR implementation. 74LS00 IC contains four 2-input NAND gates. The function table and connection diagram for this IC are shown below:

**Connection Diagram 74LS00 IC:**



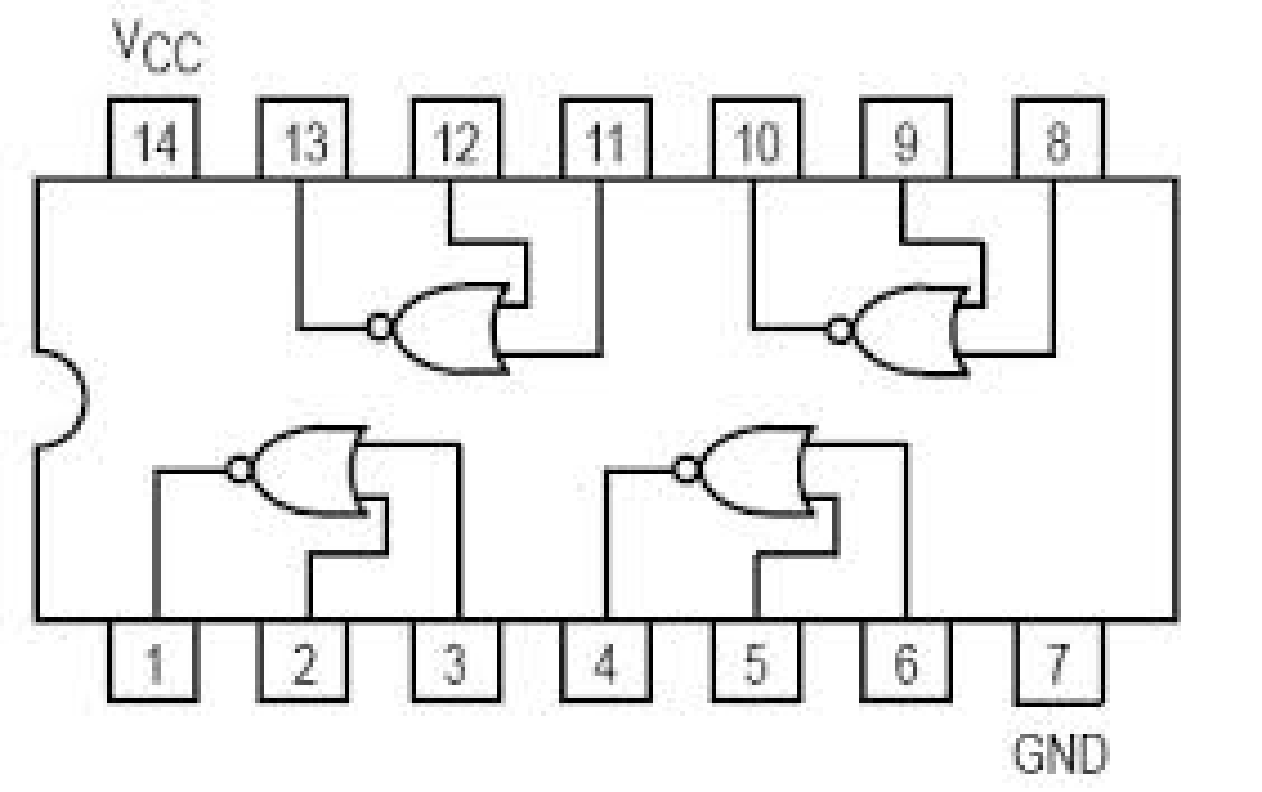
**Figure 2 : 74LS00 IC contains four 2-input NAND gates.**

**Function Table for 74LS00 IC:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Function Table: Inputs** | | **Output** | |
| **A** | **B** | | **Y** |
| L | L | | H |
| L | H | | H |
| H | L | | H |
| H | H | | L |

74LS02 IC contains four 2-input NOR gates. The function table and connection diagram for this IC are shown below:

**Connection Diagram 74LS02 IC:**



**Figure 3: 74LS02 IC contains four 2-input NOR gates**

**Function Table 74LS02 IC:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Function Table: Inputs** | | **Output** | |
| **A** | **B** | | **Y** |
| L | L | | H |
| L | H | | L |
| H | L | | L |
| H | H | | L |

**Objective:**

* To learn K-map and its usage in order to obtain cost effective circuit for implementation
* Implementation of obtained cost effect circuit on Circuit Maker and Explorer Board in order to validate the obtained circuit
* To study the realization of basic gates using universal gates (NAND gate & NOR gate)
* To learn technology mapping (NAND-NAND & NOR-NOR implementation) and its significance in order to obtain cost effective circuit for implementation

**Lab Tasks:**

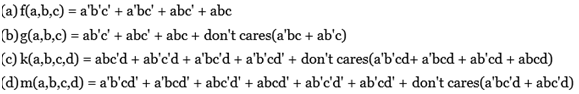
**Convert the following equations to NAND Gate, fill truth tables and implement the NAND Gate equations on the Circuit Maker and explorer board.**

1. F (A, B, C) = (A+C). (A+B)
2. F (A, B, C, D) = ABCD+ A’B’C’D’ + AB’C’D’

**Convert the following equations to NOR Gate, fill truth tables and implement the NOR Gate equations on the Circuit Maker explorer board.**

1. F (A, B, C) = (A+B). (C+B). (A+B)
2. F (A, B) = AB+ CD

**For the function listed below, determine the minimal SOP expression.**

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